CLAIMS

What is claimed is:

1. A method for detecting a page boundary in a data stream comprising:

determining a page size;

storing said page size in a binary page size register, said binary page register having a predetermined number of bits;

receiving a data stream address, said data stream address being a binary address corresponding to said data stream;

performing a Boolean logic operation on said data stream address and said page size using a Boolean logic gate to produce a binary output value;

comparing said binary output value with a predetermined binary value using a comparator; and

causing a boundary signal to change state when said output value is equal to said predetermined binary value.

2. The method of claim 1 wherein said Boolean logic operation is an AND operation.

3. The method of claim 1 wherein said Boolean logic operation is an OR operation.

4. The method of claim 1 wherein said Boolean logic operation is an XOR operation.

5. The method of claim 1 wherein said Boolean logic operation is an XNOR operation.

6. The method of claim 1 wherein said Boolean logic operation is an NOR operation.

7. The method of claim 1 wherein said Boolean logic operation is an NAND operation.

8. The method of claim 1 wherein said binary page size register is a programmable memory location.

9. The method of claim 1 wherein said Boolean logic operation, said binary page size register, and said comparator are portions of a single integrated circuit.

10. A detection circuit for detecting a page boundary in a data stream comprising:

a binary page size register having a predetermined number of bits that is capable of storing a page size;

an address input for receiving a data stream address that is a binary address corresponding to said data stream;

a Boolean logic operator having said binary page size register and said address input as inputs and a resultant output;

a binary compare register having a predetermined number of bits; and

a comparator that compares said resultant output and said binary compare register and generates a comparator output.

11. The circuit of claim 10 wherein said Boolean logic operator is an AND operation.

12. The circuit of claim 10 wherein said Boolean logic operator is an NAND operation.

13. The circuit of claim 10 wherein said Boolean logic operator is an OR operation.

14. The circuit of claim 10 wherein said Boolean logic operator is an NOR operation.

15. The circuit of claim 10 wherein said Boolean logic operator is an XOR operation.

16. The circuit of claim 10 wherein said Boolean logic operator is an XNOR operation.

17. The circuit of claim 10 wherein said binary page size register is a programmable memory location.

18. The circuit of claim 1 wherein said Boolean logic operator, said binary page size register, and said comparator are portions of a single integrated circuit.